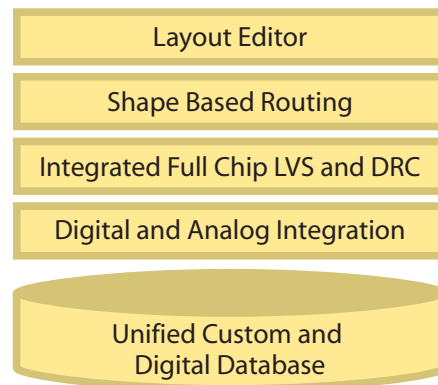


Titan™ Chip Integration and Finishing

- Includes the fastest, highest capacity and smallest memory footprint layout editing system to handle large full-chip designs.
- Full-featured custom layout editor allows all chip-finishing layout tasks such as reticle planning, critical dimension structures, alignment targets and scribe lines, flip-chip bump connections, 45-degree routing emulation and top-layer routing for the entire design.
- Analog and special-signal shape-based routing provides speed, repeatability and ease of engineering change order (ECO) implementation.
- Standard-cell digital design implemented in Talus® is fully encapsulated in Titan through a live interface, enabling designers to perform custom additions and edits to the standard-cell digital design.
- DRC and LVS checks using Quartz and other industry-standard physical verification solutions are fully encapsulated within Titan, enabling both full custom and standard-cell corrections.

Titan provides an integrated chip-finishing solution for mixed-signal designs. The unprecedented level of integration and automation provided by Titan enables significant increases in productivity by eliminating the potentially time-consuming and difficult iterations between traditional custom layout and standard-cell implementation systems. Two configurations are available. Titan Chip Integration includes a layout editor, enables complete encapsulation of the Talus® digital design solution, and integrates Quartz™ DRC and Quartz LVS verification. Titan Chip Finishing includes all of the above plus a shape-based custom router.



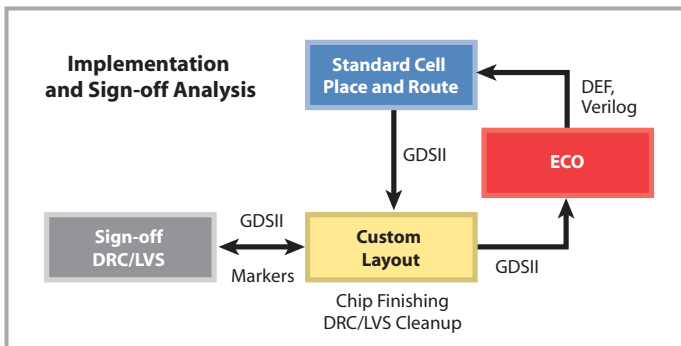
The Biggest Bottleneck to Chip Finishing

In traditional approaches, the place-and-route flow is completed after standard-cell design-rule and layout-vs.-schematic checks are clean and sign-off analysis is done. At this point, the standard-cell database has to be exported in a standard format such as GDSII and then imported into a full custom layout editor, which comprehends all the fabricated layers. The custom editor is used to add all the necessary custom layout structures for tapeout such as flip-chip bump connections, top-layer routing and reticle planning such as alignment targets and scribe lines. The complete database then has to be sent back to a sign-off DRC/LVS tool through GDSII stream-out. Violation markers must be brought back into the custom editor to perform all the needed corrections. Once this is done, all changes affecting the place-and-route areas have to be re-verified back in the place-and-route environment. Iterations back into the place-and-route system must be performed by exporting and importing data. What is worse, if an ECO is made at this stage, additional iterations are required to analyze and verify the changes made.

Titan™ Chip Integration and Finishing

Titan Eliminates the Bottleneck

Titan's live connection to Talus and tight integration with Quartz DRC and Quartz LVS completely eliminate typical iterations. Quartz DRC and Quartz LVS are directly launched from Titan. Titan's design manager automates the process of streaming out GDSII by keeping track of all references. Quartz DRC and Quartz LVS are automatically executed and their violation stepper launched when execution completes, allowing layout corrections to be performed without leaving Titan. As soon as a change is made in Titan's custom layout environment, Talus repeats sign-off checks. No database transfers are needed—standard-cell data remains in Talus in memory and custom data remains in Titan's custom environment.



The iterative loops between custom layout and standard cell digital place-and-route systems add weeks to the tapeout schedule.

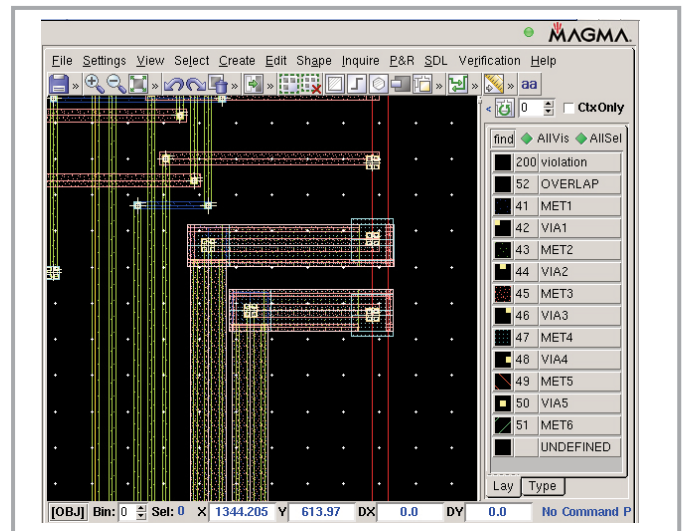
A Big Jump in Analog Routing Efficiency, Repeatability and Standardization

Similar to the leap in efficiency enabled by integration into the digital place-and-route flow, Titan is a giant step forward in automating and standardizing the routing of analog and special signals. Through an intuitive application of layout constraints, either interactively or fully automated through scripts, Titan performs bus routing, shielding, differential pair routing, star routing and other specialized routing in a matter of minutes. Existing manual approaches may take days. This becomes especially useful in the context of ECOs as rerouting can be automatically done with essentially no delay in the schedule.

TECHNOLOGY FEATURES:

Custom Layout Editor

- Comprehensive, powerful, easy-to-use feature set driven by menus and hot-keys
- Supports 100 levels of hierarchy (extendable)
- Loads large full-chip databases in minutes



Titan automatically routes co-axial shielding.

- Allows addition of rectangles, polygons, conics, paths, pins, wires, vias
- Allows shape editing including stretching, cutting, chopping, splitting, array splitting, reshaping, Boolean operations, transforming, stacking, stepping and aligning
- Allows property editing

Shape-based Router (Titan Chip Finishing only)

- Automated, constraints-driven analog and special-net routing
- Interfaces to third-party tools through OA, GDSII, LEF, DEF and Verilog
- Intuitive and easy-to-use constraints applied interactively or through Magma Tcl commands
- Bus routing includes parallel, tandem and coaxial shielding
- Differential pair, star and matched routing

Talus Integration

- Live encapsulated interface to Talus keeps Talus data current in memory with every custom layout update made in Titan
- Full set of Talus commands available from the command line or optionally by invoking the Talus GUI
- Design manager maintains references to any number of Volcano™ databases or custom blocks throughout the design hierarchy
- Connection manager allows any number of Talus sessions to be connected live and keeps track of valid Volcano databases / connections across Titan sessions

DRC / LVS Integration

- Automatic launch of Quartz DRC and Quartz LVS execution and violation stepper/browser
- Support for Quartz DRC and other industry-standard violation-marker-import for use with Titan's native violation stepper

Supported Data Formats

- GDSII, LEF, DEF, OpenAccess™, Verilog, SPICE

Supported Platforms

- Linux, Sun Solaris



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